REMARKS

Reconsideration and further examination in view of the following Remarks are requested. All objections and rejections are respectfully traversed.

Claims 1-9 and 11-18 stand rejected under 35 U.S.C. §103 as being obvious based on U.S. Pat. No. 5,956,516 to Pawlowki ("Pawlowski") in view of the PCI Local Bus Specification, Revision 2.1, June 1, 1995 ("PCI Spec."). In addition, claims 1, 12 and 15 stand rejected based on §103 based on U.S. Pat. No. 6,629,179 to Bashford ("Bashford") in view of the PCI Spec.

Claim 1

Claim 1, in relevant part, recites:

> "A method for preventing passive release of interrupts within a computer system, the computer system having at least one processor for servicing the interrupts, one or more input/output (I/O) devices configured to issue interrupts, and an I/O bridge having a plurality of ports to which I/O devices are coupled and configured to interface between the I/O devices and the processor, the method comprising the steps of:"
>
> "asserting an interrupt signal by a subject I/O device coupled to a given port of the I/O bridge",
>
> "forwarding an interrupt message corresponding to the interrupt signal to the processor for servicing",
>
> "setting an interrupt pending flag in response to assertion of the interrupt signal",
>
> "in response to the interrupt being serviced, generating a first ordered message, the first ordered message **notifying the subject I/O device that the interrupt has been serviced**",
>
> "generating a second ordered message for clearing the interrupt pending flag",

"sending the first ordered message to the given port of the I/O bridge", and

"sending the second ordered message to the given port of the I/O bridge after the first message has been sent".

The Office Action, at pp. 2-3, cites to Col. 6, lines 40-41, of Pawlowski as teaching Applicants' claimed generation and sending of a first ordered message. This excerpt states, in its entirety, as follows:

> "The SP bit is reset when the IRR bit is set. The IRR bit is set when **an interrupt message** is accepted by the processor."

Applicants submit that Pawlowski's "interrupt message" cannot be equated with the claimed "first ordered message". First of all, claim 1 specifically recites that the "first ordered message" is generated "in response to the interrupt being serviced". Second, claim 1 recites that the first ordered message "notif[ies] the subject I/O device that the interrupt **has been serviced**". In contrast, Pawlowski's "interrupt message", which is sent from the I/O host to the processor, instructs the processor to service the interrupt. Applicants direct the Examiner's attention to Col. 4, lines 35-38 and Fig. 1 of Pawlowski, which provide that the "interrupt message" described by Pawlowski is sent from the interrupt controller (34), located on Pawlowski's host bridge (16), to the processor (12). Thus, by definition Pawlowski's "interrupt message" is generated **before** the interrupt is serviced, and thus cannot possibly notify any component that the interrupt has been serviced. In contrast, as indicated above, claim 1 specifically recites that the "first ordered message" is generated in response to the interrupt being serviced, and that it notifies the subject I/O device that the interrupt has been serviced. Because Pawlowski fails to teach or suggest a first ordered message as recited in claim 1, the rejection of claim 1 based on

Pawlowski should be withdrawn. Claims 2-9 and 11, moreover, depend from claim 1 and thus they too are allowable over Pawlowski.

Claim 12

Independent claim 12, in relevant part, recites:

"A computer system comprising:"

"a plurality of input/output (I/O) devices configured to assert and deassert respective interrupt signals",

"at least one processor for servicing interrupts from the I/O devices", and

"the at least one processor, upon servicing the interrupt, sends first and second ordered messages to the given port of the I/O bridge, **the first ordered message notifying the subject I/O device that the interrupt has been serviced,** and the second ordered message clearing the interrupt pending flag".

The Office Action, at p. 4, again relies on Pawlowski's "interrupt message" as teaching or suggesting Applicants' claimed first ordered messages. Because Pawlowski's "interrupt message" provides no notification to any I/O device that an interrupt has been serviced, as explained above, the rejection of claim 12 based on Pawlowski should also be withdrawn. Claims 13-18, moreover, depend from claim 12 and thus they too are allowable over Pawlowski.

Applicants similarly submit that Bashford too fails to teach or suggest the present invention. In particular, claim 1, in relevant part, recites:

"in response to the interrupt being serviced, generating a first ordered message, the first ordered message **notifying the subject I/O device that the interrupt has been serviced**",

"generating a second ordered message for clearing the interrupt pending flag",

"sending the first ordered message to the given port of the I/O bridge", and

"sending the second ordered message to the given port of the I/O bridge after the first message has been sent".

The Office Action, at p. 6, cites to Col. 9, lines 50-64 of Bashford as teaching these limitations. This excerpt from Bashford recites as follows:

> Then in operation 1010, it is determined whether the message signaled interrupt has been sent out to the primary PCI interface 110. For example, a message signaled interrupt is sent if the primary PCI interface 110 returns a "sent" signal to the interrupt message generator 410. In such cases, the request to the PCI interface 110 is deasserted and the interrupt pending flag for the transmitted interrupt bit number is cleared in operation 1012. However, if the message signaled interrupt has not been sent out, the interrupt message generator 410 waits until it has been sent out. After clearing the interrupt pending flag, the current interrupt pointer 834 of the circular queue 408 is incremented to point to the next register location for generating the next message signaled interrupt for transmission. The method then terminates in operation 1016.

Applicants submit that, as shown, there is no teaching or suggestion by Bashford for the generation of first and second ordered messages where the first ordered message notifies the subject I/O device that the interrupt has been serviced. Instead, this excerpt of Bashford describes when a "message signaled interrupt" should be sent by a PCI bridge to a processor. Specifically, Fig. 10 of Bashford, which is the figure being described in this excerpt, is a flow chart of a method performed by Bashford's interrupt message generator (410), which is disposed on his PCI bridge. See Bashford, Col. 9, lines 20-22 and Figs. 2 and 4. A message signaled interrupt, moreover, is a mechanism by which an I/O device can request some service. See Bashford, Col. 1, lines 60-63 ("The message signaled interrupts (MSI) are essentially write transactions that enable a device to **request service** by writing a system-specified message to a system-specified address"). Because Bash-

ford's message signaled interrupt is neither generated in response to the interrupt being service nor does it notify an I/O device that the interrupt has been serviced, the rejection of claim 1 based on Bashford should be withdrawn.

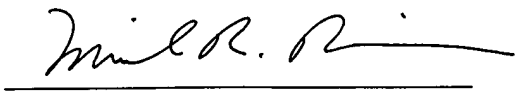
The Office Action cites to this same excerpt from Bashford in rejecting claim 12. Because Bashford's message signaled interrupt fails to teach or suggest Applicants' claimed first ordered message "for notifying the subject I/O device **that the interrupt has been serviced**", the rejection of claim 12 based on Bashford should be withdrawn. Similarly, the rejection of claim 15, which depends from claim 12, based on Bashford should also be withdrawn.

Applicants submit that the application is in condition for allowance and early favorable action is requested.

Authorization to Debit Deposit Account

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

Respectfully submitted,



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